REMARKS

Reconsideration of the present application is respectfully requested.

Summary of Office Action

The drawings stand objected to under 37 CFR 1.83(a). The Examiner states that the limitation from claims 44 and 63 "a vector processing code assembly code level . . ." must be shown in the drawings.

Claims 44-47, 49-50 and 63 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

Claims 44, 45, 49, 50 and 63 stand rejected under 35 U.S.C. § 103(a) based on U.S. Patent no. 4,766,566 of Chuang ("Chuang") in view of U.S. Patent no. 5,313,331 of Labrousse et al. ("Labrousse"), in view of U.S. Patent no. 4,766,566 of Davies ("Davies"), in view of U.S. Patent no. 4,346,437 of Blahut et al ("Blahut").

Summary of Amendments

Claims 1-43, 38 and 51-62 were previously canceled. In this amendment, claims 44 and 63 have been amended. No claims have been added or canceled. No new matter has been added.

New Figure 9 has been added to the drawings in response to the Examiner's objection that the "vector processing level" was not illustrated in the drawings. No new matter has been added.

The specification has been amended to refer to newly added Figure 9. No new matter has been added.

Discussion of Rejections

Section 112(1) Rejections

The Examiner states, "The limitation from claim 44 'A second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units' is not contained within the specification upon a cursory glance." (Office Action, p. 3). In the last amendment, Applicant identified support for this limitation at (at least) paragraphs [0044] – [0046] of the Substitute Specification filed on 10/17/2006. However, the Examiner responds, "No support is found for [this limitation] within the added paragraphs 44-46" (Office Action, p. 8).

Applicant respectfully disagrees. Support for that limitation is clearly shown in paragraphs [0044] – [0046], especially in Table 1 in paragraph [0046], which shows ALU mnemonics referring to outputs of other functional units (R, S) (see the note at the bottom of Table 1 and Fig. 3). Therefore, withdrawal of this rejection is respectfully requested.

Prior Art Rejections

Claims 44, 45, 49, 50 and 63 stand rejected under 35 U.S.C. § 103(a) based on Chuang in view of Labrousse in view of Davies in view of Blahut.

Claims 44 and 63 have been amended. Support for the amendment can be found in at least paragraph [0051] of the substitute specification.

Claim 44 now recites as follows:

44. (Currently amended) A processor comprising:

a plurality of functional units coupled to each other to execute operations defined from an instruction set of the processor, the plurality of functional units including an arithmetic logic unit (ALU) and a multiplier, the instruction set having a hierarchy of instruction levels, each of which can be used by a programmer to define instructions for the processor, the hierarchy of instruction levels including

a RISC/CISC assembly code level,

a second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units, and

a vector processing assembly code level, using which **an individual instruction** can be used to cause an operation to be automatically repeated **sequentially** a programmable number of times on different data words; and

a plurality of control registers, the plurality of hierarchical instruction levels further comprising a fourth level corresponding to the control registers, using which **individual instruction words** executed by one or more of the functional units **can be extended** by bits in the control registers on a per-instruction-cycle basis. (Emphasis added.)

To support a rejection for obviousness, the cited combination of references must teach or suggest *all of the claim limitations*. *In re Vaeck*, 947 F.2d 488, 20 USPQ.2d 1438 (Fed. Cir. 1991); MPEP § 706.02(j) (emphasis added). No combination of the cited art discloses or suggests all of the limitations of claim 44, as amended, or renders the claimed invention obvious as a whole. In particular, no combination of the cited references is seen to disclose or suggest a processor which has (among the other features):

> a vector processing assembly code level, using which **an individual instruction** can be used to cause an operation to be automatically repeated **sequentially** a programmable number of times on different data words; and
>
> a plurality of control registers, the plurality of hierarchical instruction levels further comprising a fourth level corresponding to the control registers, using which **individual instruction words** executed by one or

more of the functional units **can be extended** by bits in the control registers on a per-instruction-cycle basis. (Emphasis added.)

Similar limitations to these are also recited in claim 63.

First, regarding the "vector processing assembly code level," the Examiner contends that Davies discloses this feature at col. 17, lines 53-60 and Fig. 9a (Office Action, p. 5). What Davies discloses there is the ability to perform *SIMD* (Single Instruction Multiple Data) processing. In SIMD processing, a single instruction word is executed on multiple data subwords *in parallel* (concurrently), *not sequentially*. By contrast, with the present invention, an individual instruction can be used to cause an operation to be repeated on different data words *sequentially*. (In this regard, Applicant notes that the word "sequentially" inserted into claims 44 and 63 is considered to be redundant to the word "repeated" and has only been added to clarity the intended meaning of "repeated". Hence, this amendment is not a narrowing amendment.)

Davies does not disclose or suggest using any individual instruction to cause an operation to be repeated *(sequentially)* on different data words. Davies shows in Figure 10 that the repetition of operations is handled by an explicit conventional program loop comprising multiple instructions. Nor is such functionality found to be disclosed in any of the other cited references. For at least this reason, therefore, claims 44 and 63 and all claims which depend on them are patentable over the cited combination.

Second, regarding the "plurality of control registers" limitation, the Examiner cites Blahut at col. 8, lines 42-62 as disclosing the recited functionality (Office Action, p. 6). Blahut discloses that two bits GB1 and GB2 of the processor control register (PCR) are used to control the operand width (as 4, 8, 12 or 16 bits). Note that those two control

bits are provided to an *address decoder* (special address decoder 45), *not* to any processing unit with functionality that would otherwise use extra bits added to an instruction word. Hence, as stated by Blahut, those control bits in Blahut are used to "extend the capability of its instruction *set*" *as a whole* (see col. 8, lines 55-57)(emphasis added), *not* to extend any *individual* instruction *words* (as per claim 44), and certainly not to extend any individual instruction words on a *per-instruction-cycle basis* (per claims 44 and 63). Blahut does not disclose or suggest a plurality of control registers, where the plurality of hierarchical instruction levels further comprise a fourth level corresponding to the control registers, using which *individual instruction words* executed by one or more of the functional units can be extended by bits in the control registers on a per-instruction-cycle basis, nor is such functionality found to be disclosed in any of the other cited references. For at least this additional reason, therefore, claims 44 and 63 and all claims which depend on them are patentable over the cited combination.

Thus, no combination of the cited references discloses or suggest *all of the limitations* of claim 44 or claim 63. Therefore, claims 44 and 63 and any claims which depend on them are patentable over the cited art.

Dependent Claims

In view of the above remarks, a specific discussion of the dependent claims is considered to be unnecessary. Therefore, Applicants' silence regarding any dependent claim is not to be interpreted as agreement with, or acquiescence to, the rejection of such claim or as waiving any argument regarding that claim.

Conclusion

For the foregoing reasons, the present application is believed to be in condition for allowance, and such action is earnestly requested.

If any additional fee is required, please charge Deposit Account No. 02-2666.

Respectfully submitted,
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